REMARKS

The claims are claims 1 to 4.

The application has been amended at many locations to correct minor errors and to present uniform language throughout. These amendments include an update of the status of the copending applications cited on page 1.

A proposed drawing correction is attached. The proposed drawing correction corrects the spelling of "SYSCLK" in Figure 4 to match the text at page 11, line 10.

Claim 3 was rejected under 35 U.S.C. 112 as failing to particularly point out and distinctly claim the subject matter of the invention. The OFFICE ACTION states that the term "said monitor privilege input" appearing at line 5 and 6 has no antecedent basis.

The Examiner's attention is directed to lines 1 and 2 of claim 3. These lines state in part "wherein said integrated circuit includes a monitor privilege input." The Applicant respectfully submits this provides the required antecedence for the recitations of lines 5 and 6.

Claims 1 to 4 were rejected under 35 U.S.C. 102(e) as anticipated by Deao et al., U.S. Patent No. 6,055,649. The OFFICE ACTION states at paragraph 6 spanning pages 3 and 4:

> "As per claim 1, Deao anticipates method of in-circuit emulation of an integrated circuit with feature limitation very identical to the claimed invention (Abstract and Summary of the Invention). According to Deao, the in-circuit emulation method includes steps of detecting predetermined debug events for debug mechanism (col. 25, lines 27-46, cols. 42-43, for example), upon detection of debug stage or event suspending program execution except for at least one type interrupt, and executing an emulation monitor program via the at least one type of interrupt as claimed (cols. 45, 46, 50-54, for example).

> "As per claim 2, Deao discloses serial scan path, and assigning selective emulation resource to serial scan path of the monitor program (cols. 55-61, for instance).
> "As per claim 3, Deao discloses resource sharing including prioritizing resources, privilege resources, etc. for optimizing the performance.
> "As per claim 4, Deao discloses read and write scan registers, and assigning such registers to emulate circuit operation as claimed."

The Applicant respectfully submits that the OFFICE ACTION fails to meet the requirements of 37 CFR §1.106(b). The text of 37 CFR §1.106(b) states:

> "(b) In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified."

The application of the teachings of Deao above quoted to claims 1 to 4 fails to satisfy the requirements of 37 CFR §1.106(b). Regarding the step of suspending program execution except for at least one type interrupt on detection of a debug event and execution of an emulation monitor program via such an interrupt, the OFFICE ACTION cites seven columns of Deao et al. Regarding claim 2, the OFFICE ACTION likewise cites seven column of Deao et al. The reference Deao et al consisting of 32 sheets of drawings and more than 82 columns of text is both complex and shows inventions other that those of claims 1 to 4 of this application. If these limitations are taught in Deao et al, it should be possible to designate particular parts of less than seven columns of text regarding two limitations of claim 1 and a single limitation of claim 2. The pertinence of these parts of Deao et al with regard to these limitations is not apparent to this attorney.

Note further that the OFFICE ACTION fails even to attempt to point out parts of Deao et al relevant to the limitations of claims 3 and 4.

The Applicant respectfully requests a more detailed application of the teachings of the cited references to the features of the claims. The Applicant would greatly appreciate citation of individual reference numbers illustrated in the references for each claimed element. In addition, it would greatly help the Applicant to limit citations to the text of the references to no more than 10 to 15 lines. The Applicant believes that it is the duty of the Examiner under 37 CFR §1.106(b) to provide such detail.

Claim 1 recites subject matter not anticipated in Deao et al. Claim 1 recites "upon detection of said predetermined debug event suspending program execution except for at least one type interrupt." The Applicant respectfully submits that Deao et al discloses detecting debug events, but fails to teach suspension of program execution except for certain interrupts as claimed. The portion of Deao et al cited in the OFFICE ACTION does not teach this limitation. Accordingly, claim 1 is allowable over Deao et al.

Claim 1 recites further subject matter not anticipated in Deao et al. Claim 1 recites "executing an emulation monitor program via said at least one type interrupt." The Applicant respectfully submits that Deao et al fails to disclose this manner of executing an emulation monitor program. The portion of Deao et al cited in the OFFICE ACTION does not teach this limitation. Accordingly, claim 1 is allowable over Deao et al.

Claim 2 recites subject matter not anticipated in Deao et al. Claim 2 recites "selectively assigning at least one emulation resource of the integrated circuit to one of said serial scan path or said monitor program." The Applicant respectfully submits that Deao et al discloses a serial scan path, but fails to teach

selective allocation of an emulation resource to the serial scan path of the monitor program. The portion of Deao et al cited in the OFFICE ACTION does not teach this limitation. Accordingly, claim 2 is allowable over Deao et al.

Claim 3 recites subject matter not anticipated by Deao et al. Claim 3 recites a monitor privilege input and further recites that the selective assigning of emulation resources is based upon a digital state of the monitor privilege input. The Applicant respectfully submits that Deao et al fails to disclose this manner of assigning an emulation resource. The portion of Deao et al cited in the OFFICE ACTION does not teach this limitation. Accordingly, claim 3 is allowable over Deao et al.

Claim 4 recites subject matter not anticipated by Deao et al. Claim 4 recites a read write data register and further recites that the selective assigning of emulation resources includes accessing this read write data register. The Applicant respectfully submits that Deao et al fails to disclose this manner of assigning an emulation resource. The portion of Deao et al cited in the OFFICE ACTION does not teach this limitation. Accordingly, claim 4 is allowable over Deao et al.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Note inserted text is marked by underlining and deleted text is marked by ~~strikeout~~.

In the Specification

Rewrite the paragraph at page 1, lines 4 to 5 as follows:

--U.S. Patent Application Serial Number 09/154,385 entitled "METHOD OF INITIALIZING A CPU CORE FOR EMULATION" filed September 16, 1998, now U.S. Patent Number 6,167,365 granted December 26, 2002; and--

Rewrite the paragraph at page 1, lines 7 to 9 as follows:

--U.S. Patent Application Serial Number ~~(TI-28928P)~~ 09/483,367, entitled "EMULATION SUSPEND MODE WITH DIFFERING RESPONSE TO DIFFERING CLASSES OF INTERRUPTS" claiming priority from U.S. Provisional Application No. 60/120,809 filed February 19, 1999;--

Rewrite the paragraph at page 1, lines 10 to 11 as follows:

--U.S. Patent Application Serial Number ~~(TI-28929P)~~ 09/481,852, entitled "EMULATION SUSPENSION MODE WITH STOP MODE EXTENSION" claiming priority from U.S. Provisional Application No. 60/120,809 filed February 19, 1999;--

Rewrite the paragraph at page 1, lines 12 to 13 as follows:

--U.S. Patent Application Serial Number ~~(TI-28930P)~~ 09/483,568, entitled "EMULATION SUSPEND MODE HANDLING MULTIPLE STOPS AND STARTS" claiming priority from U.S. Provisional Application No. 60/120,809 filed February 19, 1999;--

Rewrite the paragraph at page 1, lines 14 to 15 as follows:

--U.S. Patent Application Serial Number ~~(TI-28931P)~~ 06/09/483,697, entitled "EMULATION SUSPEND MODE WITH FRAME CONTROLLED RESOURCE ACCESS " claiming priority from U.S. Provisional Application No. 60/120,809 filed February 19, 1999;--

Rewrite the paragraph at page 1, lines 16 to 17 as follows:

--U.S. Patent Application Serial Number ~~(TI-28932P)~~ 09/482,902, entitled "EMULATION SUSPEND MODE WITH INSTRUCTION JAMMING" claiming priority from U.S. Provisional Application No. 60/120,809 filed February 19, 1999;--

Rewrite the paragraph at page 1, lines 18 to 20 as follows:

--U.S. Patent Application Serial Number ~~(TI-28934P)~~ 09/483,237, entitled "EMULATION SYSTEM WITH SEARCH AND IDENTIFICATION OF OPTIONAL EMULATION PERIPHERALS" claiming priority from U.S. Provisional Application No. 60/120,960 filed February 19, 1999;--

Rewrite the paragraph at page 1, lines 21 to 23 as follows:

--U.S. Patent Application Serial Number ~~(TI-28935P)~~ 09/483,783, entitled "EMULATION SYSTEM WITH ADDRESS COMPARISON UNIT AND DATA COMPARISON UNIT OWNERSHIP ARBITRATION" claiming priority from U.S. Provisional Application No. 60/120,791 filed February 19, 1999;--

Rewrite the paragraph at page 1, lines 24 to 26 as follows:

--U.S. Patent Application Serial Number ~~(TI-28936P)~~ 09/481,853, entitled "EMULATION SYSTEM WITH PERIPHERALS RECORDING EMULATION FRAME WHEN STOP GENERATED" claiming priority from U.S. Provisional Application No. 60/120,810 filed February 19, 1999; and--

Rewrite the paragraph at page 1, lines 27 to 29 as follows:

--U.S. Patent Application Serial Number ~~(TI-28937P)~~ 09/483,321, entitled "EMULATION SYSTEM EMPLOYING SERIAL TEST PORT AND ALTERNATIVE DATA TRANSFER PROTOCOL~~.~~" claiming priority from U.S. Provisional Application No. 60/120,667 filed February 19, 1999.--

Rewrite the paragraph at page 7, lines 14 to 19 as follows:

--Debug host computer 1 consists of a computer, for example a PC, running a CPU core specific software debugger as one of its tasks. The debug host computer 1 allows the user to issue high level commands such as setting ~~breakpoint~~ breakpoints, single stepping the programmable digital processor in target system 3 and displaying the contents of a memory range.--

Rewrite the paragraph at page 10, lines 6 to 17 as follows:

--The preferred embodiment of this invention includes an extension to the JTAG interface. Two pins nET0 and nET1 serve as a two pin trigger channel function. This function supplements the serial access capability of the standard interface with continuous monitoring of device activity. The two added pins create debug and test capabilities that cannot be created with the standard interface. The nET0 signal is called Emulation and Test 0 Not. This signal helps create a trigger to channel zero. Similarly, the nET1 signal is called Emulation and Test ~~0~~ 1 Not. This signal helps create a trigger to channel one. These channels will be further explained below.--

Rewrite the paragraph at page 11, lines 3 to 16 as follows:

--Figure 4 illustrates an electrical connection view of the coupling between access adapter 2 and target system 3. Figure 4 shows the connections of the of the various signals of the JTAG

header 5 illustrated in Figure 2. All these signals are connected to scan controller 41. The signals nTRST, TCK and TMS are connected to two example megamodules 31 and 33. Figure 4 illustrates the optional connection of TCKO to the target system clock SYSCLK. The scan input TDI connects to a scan input of megamodule 31. The scan output of megamodule 31 supplies the scan input of eg module 33. The scan output of ~~meg module~~ megamodule 33 supplies the scan output TDO. The two extension signals nET0 and nET1 control meg modules 31 and 33 via merge unit 32. These extension signals are monitored by test equipment 43.--

Rewrite the paragraph at page 11, lines 17 to 24 as follows:

--The debugging environment illustrated in Figures 1 to 4 permit the user to control application execution by any programmable digital processor of target system 3. Typical control processes include: keyboard directives such as run, halt and step; software ~~breakpoint~~ breakpoints using op-code replacement; internal analysis ~~breakpoint~~ breakpoints specified by the program counter or watchpoints specified by data accesses; and externally generated debug events.--

Rewrite the paragraph at page 11, line 25 to page 12, line 2 as follows:

--Actions such as decoding a software breakpoint instruction (DSTOP), the occurrence of an analysis breakpoint or watchpoint (ASTOP), or the occurrence of a debug host computer event (HSTOP) are referred to as debug events. Debug events cause execution to suspend. Debug events tied to the execution of specific instructions are called ~~breakpoint~~ breakpoints. Debug events generated by memory references are called watchpoints. External debug events can also suspend execution. Debug events cause entry into the Debug State.--

Rewrite the paragraph at page 12, line 17 to page 13, line 2 as follows:

--The operational state transits from execute state 101 to debug suspend state 102 upon a debug event. The debugging environment of the preferred embodiment of this invention allows the suspension of program execution at points defined by ~~breakpoint~~ breakpoints, watchpoints, and debug software directives, provided the application is an allowable debug suspend window. In general, debug events are allowed at an instruction boundary, when reset is inactive and no interrupts are active. Program execution suspends at an instruction boundary and the operational state changes to debug suspend state 102. When any debug condition is not met, the operational state remains in execute state 101 and no debug event processing occurs. The debugging environment permits debug event processing in the delayed slots of delayed branch instructions. Debug events occurring outside the debug suspend window create a debug pending condition. This condition suspends program execution when the application enables debug interrupts by opening the debug suspend window.--

Rewrite the paragraph at page 13, line 26 to page 14, line 5 as follows:

--Certain interrupts ~~transit~~ transition the operation state from debug suspend state 102 to interrupt during suspend (IDS) state 103. These interrupts are defined by a separate interrupt mask independent of the normal interrupt mask. Those interrupts defined as high priority interrupts (HPI) or foreground interrupts cause the operation state to enter the interrupt during suspend state 103 from the debug suspend state 102. The debug suspend state 102 enables high priority interrupts independent of the state of the global interrupt enable bit or of software run directives. This enables debugging of background tasks while the target device 3

continues to service a real time application via high priority interrupts.--

Rewrite the paragraph at page 15, lines 1 to 9as follows:

--The digital frame counter is decremented upon each return from interrupt. This count permits the debug environment to track the status of the suspended foreground task. For example, a taken high priority interrupt may change the machine state and thus the current machine state would not reflect the suspended background task. However, if the digital frame counter were zero, then the debug environment is assured no interrupts have ~~not~~ temporarily changed the machine state.--